II. REMARKS

Claims 1-27 are pending. The Applicants' attorney has amended claims 1, 9, 16-18, and 23, and has added new independent claims 28 and 29. But the amendments to claims 1, 9, 17-18, and 23 do not narrow these claims. All of the currently pending claims are in condition for allowance, and the Applicants' attorney requests the Examiner to withdraw all of the outstanding rejections. **But if after considering this response the Examiner does not allow all the claims, the Applicant's attorney requests that the Examiner contact him to schedule and conduct a telephone interview before issuing a subsequent Office Action.**

Rejection Of Claims 1-27 Under 35 U.S.C. § 112, Second Paragraph

The Applicant's attorney has amended the claims to overcome this rejection. These amendments, however, do not alter the intended meanings of the claims as previously discussed with the Examiner, and thus do not raise new issues that would require a further search or further consideration by the Examiner.

Rejection of Claims 1-2, 5-8, and 16 Under 35 U.S.C. § 102(b) As Being Anticipated By U.S. 6,112,288 To Ullner

The Applicants' attorney requests the Examiner to withdraw this rejection for the reasons set forth below.

Claim 1

Claim 1 as amended recites a host processor operable to execute a program instruction, and a pipeline accelerator coupled to the host processor and operable to generate data without executing any program instruction.

For example, referring, *e.g.,* to FIG. 3 and paragraphs [46], [49], and [68], an embodiment of a peer-vector machine 40 includes a host processor 42 operable to execute a program instruction stored in a memory 66, and includes a pipeline accelerator 44 operable to generate data without executing any program instruction. That is, similar to the mathematical operations that a hand-held calculator performs, the operations that an embodiment of the pipeline accelerator 44 performs are "burned" or "hardwired" into the accelerator's circuitry, which may include combinatorial logic, sequential logic, state machines, and other types of non-instruction-executing circuitry. By not executing programming instructions, the pipeline accelerator 44 can often generate data at a rate faster than an instruction-executing processor can for a given clock frequency.

In contrast, referring, *e.g.,* to Ullner's FIGS. 3-4 and col. 5 lines 32-58, Ullner does not disclose a pipeline accelerator operable to generate data without executing any program instruction. Ullner's accelerator chips 43, which compose Ullner's accelerator hardware 19, must execute program instructions to generate data. Specifically, each accelerator chip 43 includes an instruction processor 51 and an instruction distribution unit 61b, which distributes program instructions to the pipeline processors 53.

Referring to FIG. 8 and col. 8, lines 19-23 of Ullner, the Examiner seems to believe that the mode decoder 81 generates data (presumably signals S0 – S7) without executing a program instruction.

But the Applicants' attorney disagrees. First, the mode decoder 81 is not a pipeline accelerator. Second, even if, for the sake of argument, the mode decoder 81 is a pipeline accelerator, the mode decoder 18 generates the signals S0 – S7 by decoding a program instruction provided via the program-instruction decoder 78. Consequently, the mode decoder 18 does not generate data without executing any program instruction.

Claims 2 and 5-8

These claims are patentable by virtue of their dependencies from claim 1.

Claim 16

Claim 16 as amended recites a host processor operable to generate host data, and a pipeline accelerator operable to generate pipeline data from the host data without executing any program instruction, and operable to provide the pipeline data to a destination remote from the pipeline accelerator.

For example, referring to FIG. 3 of the patent application, the pipeline accelerator 44 is operable to generate pipeline data without executing any program instruction and is operable to provide the pipeline data to the host processor 42 or to another destination remote from the pipeline accelerator.

Therefore, claim 16 is patentable for reasons similar to those discussed above in support of the patentability of claim 1.

Furthermore, even if, for the sake of argument, Ullner's decoder 81 (Ullner's FIG. 8) generates the signals S0 – S7 without executing any program instruction, Ullner includes no disclosure of the decoder 81 providing these signals to a destination remote from accelerator chip 43 (Ullner's FIG. 3) on which it is disposed.

Rejection of Claims 1-4, 9-12, 18, 20-21, 23, 25, and 26 Under 35 U.S.C. § 102(e) As Being Anticipated By U.S. 2002/0087829 To Snyder et al.

The Applicants' attorney requests the Examiner to withdraw this rejection for the reasons set forth below.

Claim 1

Claim 1 as amended recites a pipeline accelerator coupled to a host processor and operable to generate data without executing any program instruction.

In contrast, referring, *e.g.*, to Snyder's FIGS. 1-2 and 4 and paragraph [0022], Snyder does not disclose a pipeline accelerator operable to generate data without executing any program instruction. As understood by the Applicants' attorney, Snyder's complex arithmetic elements (CAEs of FIG. 2), which compose Snyder's scaleable functional units (SFUs) 106 (FIG. 1), must execute program instructions to generate data. Specifically, referring to FIG. 4, each CAE includes a sequencer 400, which receives and executes program instructions and which controls the operations of an arithmetic unit 404 in response to the program instructions.

Referring to Snyder's FIG. 4, the Examiner seems to believe that Snyder's sequencer 400 does not execute program instructions.

But the Applicants' attorney disagrees. As understood by the Applicants' attorney, the sequencer 400 decodes an op-code portion of a programming instruction into control information, which causes the arithmetic unit 404 to perform an operation specified by the op-code. The sequencer 400 also decodes a data-address portion of the programming instruction, and provides the decoded address to a memory 402, which provides the addressed data to the arithmetic unit 404. In this way, the sequencer 400 causes the unit 404 to perform on the addressed data the operation specified by the op-code. Consequently, contrary to the Examiner's assertion, Snyder's CAEs (FIG. 2) do not generate data without executing any program instruction.

Claims 2-4

These claims are patentable by virtue of their dependencies from claim 1.

Claim 9

Claim 9 as amended is patentable for reasons similar to those discussed above in support of the patentability of claim 1 over Snyder.

Claims 10-12

These claims are patentable by virtue of their dependencies from claim 9.

Claim 18

Claim 18 as amended is patentable for reasons similar to those discussed above in support of the patentability of claim 1 over Snyder.

Claims 20-21

These claims are patentable by virtue of their dependencies from claim 18.

Claim 23

Claim 23 as amended is patentable for reasons similar to those discussed above in support of the patentability of claim 1 over Snyder.

Claims 25-26

These claims are patentable by virtue of their dependencies from claim 23.

Rejection of Claims 13-15, 17, 19, 22, 24, and 27 Under 35 U.S.C. § 103(a) As Being Unpatentable Over Snyder In View Of Ullner

The Applicants' attorney requests the Examiner to withdraw this rejection for the reasons set forth below.

Claims 13-15

These claims are patentable by virtue of their dependencies from claim 9.

Claim 17

Claim 17 as amended recites a pipeline accelerator operable to generate data without executing any program instruction.

Per above, neither Snyder nor Ullner discloses or suggests a pipeline accelerator operable to generate data without executing any program instruction. Consequently, the combination of Snyder and Ullner does not suggest a pipeline accelerator operable to generate data without executing any program instruction.

Claims 19 and 22

These claims are patentable by virtue of their dependencies from claim 18.

Claims 24 and 27

These claims are patentable by virtue of their dependencies from claim 23.

Conclusion

In light of the foregoing, claims 2-8, 10-15, 19-22, and 24-27 a previously pending, claims 1, 9, 16-18, and 23 as amended, and new claims 28-29 are in condition for allowance, which is respectfully requested.

In the event additional fees are due as a result of this amendment, payment for those fees has been enclosed in the form of a check. Should further payment be required to cover such fees you are hereby authorized to charge such payment to Deposit Account No. 07-1897.

DATED this 7th day of December, 2006.

Respectfully Submitted,

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